REMARKS

The Applicants make the forgoing amendments to place the Claims in condition for allowance, or alternatively, to frame the issues for appeal. In response to the Examiner's Action mailed June 20, 2001, Applicants have amended Claims 1,12 and 24 and canceled Claims 2 and 14. These amendments should not necessitate a new search because the subject matter added to independent Claims 1, 12, 24, previously appeared in dependent Claims 2 and 13 submitted with the original application. Accordingly, Claims 1, 4-12 and 15-24 are currently pending in the application.

I. Rejection of Claims 1, 2, 4-12 and 15-24 under 35 U.S.C. §103

The Examiner has rejected Claims 1, 4-12 and 15-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,604,156 to Chung, *et. al.* (Chung) in view of U.S. Patent 5,731,225 to Yamamori (Yamamori). The Applicants respectfully maintain that the claimed invention is not obvious in view of the foregoing references, and that the Examiner has failed to establish a *prima facie* case of obviousness of Claims 1, 4-12 and 15-24.

As acknowledged by the Examiner, Chung fails to disclose "wherein the contact plug is subject to a temperature sufficient to anneal the barrier layer." (Examiner's Detailed Action mailed January 31, 2001, page 2, lines 16-17). To address this deficiency, the Examiner asserts that Yamamori teaches "subjecting the contact plug to a temperature sufficient to anneal the barrier layer in order to remove the halogen containing grains . . . ." (Examiner's Detailed Action mailed January 31, 2001, page 3, lines 10-11).

Yamamori, however, states that the process by which fluorine is removed "is not fully understood" but may involve "chemical action." (Column 4, Lines 26-28). Yamamori is directed

to providing a method to remove fluorine from a TiN film. (Column 2, Lines 44-54). Yamamori achieves this though the use of a four-chambered device shown in FIGURE 3. Chamber 3 is used to etch back a blanket tungsten layer 16, exposing the surface of the TiN film 15. (Column 4, Lines 5-9; FIGURE 1D). The wafer is then transferred to Chamber 4, via vacuum Chamber 2. (Column 4, Lines 12-16; FIGURE 3). Fluorine is then "removed by setting the treatment pressure . . . to 0.3 Torr or lower, raising the wafer temperature to 220° C, or higher, and blowing nitrogen on the wafer surface for 20 sec or more." (Column 4, Lines 19-24).

The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to subject the contact plug of Chung to a temperature sufficient to anneal the barrier layer as in Yamamori. The Examiner contends that this follows because the Yamamori teaches that halogen-containing etchants result in the formation of grains that inhibit "subsequently materials from being deposited on a smooth surface and being processed optimally." (Examiner's Detailed Action mailed January 31, 2001, page 2, lines 16-17). The Applicants respectfully disagree.

The asserted combination of Chung with Yamamori fails to establish a *prima facie* case of obviousness because the combination of these two references is improper. The combination of Chung with Yamamori is improper because a person having ordinary skill in the art would not be motivated to find or add to Chung the teachings and suggestions of Yamamori, inasmuch as Yamamori does not address the problem of formation of protrusions arising because of the different etching rates for insulating as compared to capping layers. One having ordinary skill in the art would not be motivated to apply Yamamori to Chung because Chung's CMP step(s) entirely removes the wire and barrier layer to expose the first insulating layer (FIGUREs 2D and 3B). Thus, Chung is not

concerned with the deposition of fluorine grains or with their effect on the processing of subsequently deposited material. It follows therefore that there would be no motive to insert Chung's wafer into Yamamori's fourth chamber to remove fluorine.

Moreover, the Applicants respectfully maintain that there is no teaching or suggestion of annealing that can be attributed to Yamamori. The Examiner submits that "Yamamori taught heating (i.e., annealing) to a temperature of 220° C or higher clearly suggests a process of annealing the barrier layer as far as the invention defined by the instantly presented claims is concerned." (Examiner's Detailed Action mailed June 6, 20, 2001, page 3, lines 14-16). In response, the Applicants have amended Claim 1 to clarify that the claimed invention refers to a temperature sufficient to anneal said barrier layer where said barrier layer includes "a titanium layer and depositing a titanium nitride layer on said titanium layer" (Claim 1, lines 4-5).

Neither Chung nor Yamamori, provide any teaching or suggestion of annealing as define in amended Claim 1. Moreover, Yamamori expressly states that he does not fully understand the process by which fluorine is removed, but believes this occurs by chemical action. Yamamori also makes clear that the purpose of heating to a temperature of 220° C or higher is "to thereby remove fluorine from said surface of said barrier layer without etching said barrier layer." (Column 6, lines 17-19 and lines 35-37).

The Applicants respectfully submit that a temperature sufficient to remove fluorine from a barrier layer is inherently insufficient to anneal the barrier layer, when the barrier layer includes a titanium and a titanium nitride layer on said titanium layer. Annealing traditionally refers to raising and maintaining the temperature of glass or metal to a specificed temperature sufficient to remove internal strains, distortions and imperfections. *See* Richard J. Lewis, CONDENSED CHEMICAL

DICTIONARY 78 (13th ed. John Wiley & Sons, Inc., 1997). Yamamori would have no motivation to exceed his thermal budget to raise the temperature beyond a temperature needed to remove fluorine from the barrier layer. Thus, one practicing Yamamori's invention would never reach a temperature sufficient to anneal the barrier layer. Rather, it only through the improper use of hindsight that one may arrive at the claimed invention out of the isolated teachings of Chung and Yamamori or their combination. Therefore Yamamori, alone or in combination with Chung fails to teach or suggest all elements of the invention in amended Claim 1.

Because Chung and Yamamori are not properly combined and fail to teach or suggest all elements of the claimed invention, they fail to establish a *prima facie* case of obviousness with respect to Claim 1 and its dependent Claims 4-11.

And because the limitations of independent Claims 12 and 24 are analogous to those of Claim 1, the combination of Chung and Yamamori has therefore also failed to make a *prima facie* case of obviousness with respect to these claims as well as dependent Claims 15-23.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 1, 4-12 and 15-24 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

II. Conclusion

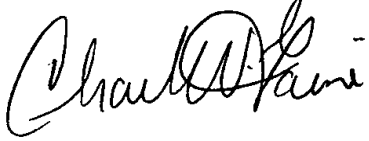
In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1, 4-12 and 15-24.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



Charles W. Gaines
Registration No. 36,804

Dated: 8/17/01

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800

Email: cgaines@abstractassets.com

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1. (Twice Amended) A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

(2) Kindly cancel Claim 2 without prejudice or disclaimer.

(3) Kindly amend Claim 12 as follows:

12. (Twice Amended) A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

(4) Kindly cancel Claim 14 without prejudice or disclaimer.

(5) Kindly amend Claim 24 as follows:

24. (Amended) A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.